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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H01L

A2

(11) International Publication Number: WO 00/51167

(43) International Publication Date: 31 August 2000 (31.08.00)

(21) International Application Number: PCT/US00/03664

(22) International Filing Date: 10 February 2000 (10.02.00)

(30) Priority Data:
09/267,921 26 February 1999 (26.02.99) US

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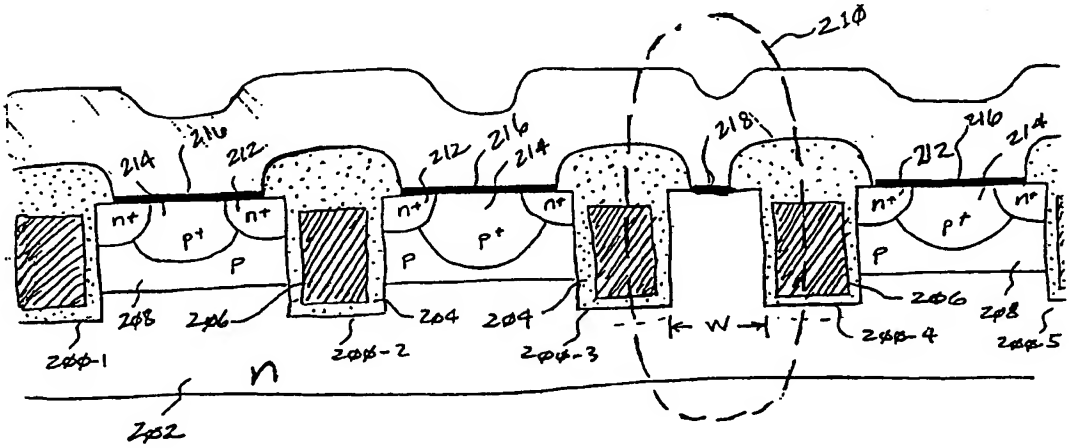
(81) Designated States: JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: MONOLITHICALLY INTEGRATED TRENCH MOSFET AND SCHOTTKY DIODE



(57) Abstract

A monolithically integrated Schottky diode together with a high performance trenched gate MOSFET. A MOS enhanced Schottky diode structure is interspersed throughout the trench MOSFET cell array to enhance the performance characteristics of the MOSFET switch. The forward voltage drop is reduced by taking advantage of the low barrier height of the Schottky structure. In a specific embodiment, the width of the trench is adjusted such that depletion in the drift region of the Schottky is influenced and controlled by the adjacent MOS structure to increase the reverse voltage capability of the Schottky diode.

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MONOLITHICALLY INTEGRATED TRENCH MOSFET AND SCHOTTKY DIODE

BACKGROUND OF THE INVENTION

The present invention relates in general to semiconductor technology, and in particular to a semiconductor device with a monolithically integrated trenched gate MOSFET and SCHOTTKY diode, and its method of manufacture.

In today's electronic devices it is common to find the use of multiple power supply ranges. For example, in some applications, central processing units are designed to operate with a different supply voltage at a particular time depending on the computing load. Consequently, dc/dc converters have proliferated in electronics to satisfy the wide ranging power supply needs of the circuitry. Common dc/dc converters utilize high efficiency switches typically implemented by power MOSFETs such as those manufactured by Fairchild Semiconductor. The power switch is controlled to deliver regulated quanta of energy to the load using, for example, a pulse width modulated (PWM) methodology.

Referring to Figure 1, there is shown a simplified circuit schematic for a conventional dc/dc converter. A PWM controller 100 drives the gate terminals of a pair of power MOSFETs Q1 and Q2 to regulate the delivery of charge to the load. MOSFET switch Q2 is used in the circuit as a synchronous rectifier. In order to avoid shoot-through current, both switches must be off

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SUMMARY OF THE INVENTION

The present invention provides methods and structures for monolithic integration of a Schottky diode together with a high performance trenched gate MOSFET. Broadly, this invention intersperses a MOS enhanced Schottky diode structure throughout the trench MOSFET cell array to enhance the performance characteristics of the MOSFET switch. The forward voltage drop is reduced by taking advantage of the low barrier height of the Schottky structure. In addition, this diode will have an inherent reverse recovery speed advantage compared to the normal pn junction of the vertical power MOSFET. The invention uses features of the trench process to optimize the performance of the Schottky diode. In a specific embodiment, the width of the trench is adjusted such that depletion in the drift region of the Schottky is influenced and controlled by the adjacent MOS structure to increase the reverse voltage capability of the Schottky diode.

Accordingly, in one embodiment, the present invention provides a monolithically integrated structure combining a field effect transistor and a Schottky diode on a semiconductor substrate, including: a trench extending into the substrate and forming a gate electrode of the field effect transistor; a pair of doped source regions positioned adjacent to and on opposite sides of the trench and inside a doped body region, the doped source regions forming a source electrode of the field effect transistor and the substrate forming a drain electrode of the field effect transistor; and a Schottky diode having a barrier layer formed on the surface of the substrate and between a pair of adjacent diode trenches extending into the substrate, the pair of adjacent diode trenches being separated by a distance W.

In another embodiment, the present invention provides a monolithically integrated structure combining a field effect transistor and a Schottky diode on a semiconductor substrate, including: first and second trenches

present invention may be gained with reference to the detailed description below and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a simplified circuit schematic for a dc/dc converter using power MOSFETs with a Schottky diode;

Figure 2 shows a cross-sectional view of an exemplary embodiment for the integrated trench MOSFET-Schottky diode structure according to the present invention;

Figure 3 shows a cross-sectional view of another exemplary embodiment for the integrated trench MOSFET-Schottky diode structure according to the present invention;

Figure 4 is a cross-sectional view of yet anther exemplary embodiment for the integrated trench MOSFET-Schottky diode structure according to the present invention;

Figures 5A and 5B show top views of the integrated trench MOSFET-Schottky diode structure for the embodiments shown in Figures 2 and 3, respectively, assuming an exemplary open-cell trench MOSFET process;

Figure 6 shows a different embodiment for the integrated trench MOSFET-Schottky diode structure of the present invention wherein the Schottky diode is interspersed alternately in parallel with the longitudinal axis of the trenches in an exemplary open-cell trench process; and

Figures 7A and 7B show top view of two alternative embodiments for the structure shown in Figure 6.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

Referring to Figure 2, there is shown a cross-sectional view of a simplified example of an integrated trench MOSFET-Schottky diode structure fabricated on a silicon substrate 202 according to the present invention. A plurality of trenches 200 are patterned and etched into substrate 202. Substrate 202 may comprise an n-type epitaxial upper layer (not shown). A thin layer of dielectric 204 (e.g., silicon dioxide) is formed along the walls of trenches 200, after which conductive material 206 such as polysilicon is deposited to substantially fill each trench 200. A p-type well 208 is then formed between trenches 200 except between those trenches (e.g., 200-3 and 200-4) where a Schottky diode is to be formed. Thus, the regions 210 between trenches 200-3 and 200-4 where a Schottky diode is to be formed is masked during the p-well implant step. N+ source junctions 212 are then formed inside p-well regions 208, either before or after the formation of a p+ heavy body regions 214. A layer of conductive material 216 such as titanium tungsten (TiW) or titanium nitride (TiNi) is then patterned and deposited on the surface of the substrate to make contact to n+ source junctions 212. The same material is used in the same step to form anode 218 of Schottky diode 210. Metal (e.g., aluminum) is then deposited on top to separately contact MOSFET source regions 212 as well as p+ heavy body 216 and Schottky anode 218. A preferred process for the trench MOSFET of the type shown in the exemplary embodiment of Figure 2, is described in greater detail in commonly-assigned U.S. patent application number 08/970,221, titled "Field Effect Transistor and Method of its Manufacture," by Bencuya et al., which is hereby incorporated by reference in its entirety. It is to be understood, however, that the teachings of the present invention apply to other types of trench processes

with, for example, different body structures or trench depths, different polarity implants, closed or open cell structures, etc.

The resulting structure, as shown in Figure 2, includes a Schottky diode 210 that is formed between two trenches 200-3 and 200-4 surrounded by trench MOSFET devices on either side. N-type substrate 202 forms the cathode terminal of Schottky diode 210 as well as the drain terminal of the trench MOSFET (see Figure 1). Conductive layer 218 provides the diode anode terminal that connects to the source terminal of the trench MOSFET. In this embodiment, the polysilicon in trenches 200-3 and 200-4 connects to the gate polysilicon (206) of the trench MOSFET and is therefore similarly driven. The Schottky diode as thus formed has several operational advantages. As voltage builds on the cathode of the Schottky diode (i.e., substrate 202), the MOS structure formed by the poly filled trenches 200-3 and 200-4 forms a depletion region. This helps reduce the diode leakage current. Furthermore, the distance W between trenches 200-3 and 200-4 can be adjusted such that the growing depletion regions around each trench 200-3 and 200-4 overlap in the middle. This pinches off the drift region between Schottky barrier 218 and the underlying substrate 202. The net effect is a significant increase in the reverse voltage capability of the Schottky diode with little or no detrimental impact on its forward conduction capability.

In a preferred embodiment, the distance W between trenches 200-3 and 200-4, or the width of the mesa wherein the Schottky diode is formed, is smaller than inter-trench spacing for MOSFETs. The distance W can be, for example, 0.5 μm depending on doping in the drift region and the gate oxide thickness. The opening in which anode contact 218 is formed is even smaller than W, which may test the limits of the manufacturing process. To allow for greater manufacturing process flexibility, the present invention provides an alternate embodiment in Figure 3. Referring to Figure 3, a trench MOSFET-Schottky diode structure is shown that is similar to that shown in Figure 2 except for two

variations. The first variation relates to facilitating the manufacturing process by enlarging the anode contact area. This is accomplished by isolating the polysilicon layers (302-2, 302-3, 302-4) inside the trenches between which the Schottky diode is formed, from the gate polysilicon layers for the trench MOSFET devices. These isolated trench polysilicon layers (302-2, 302-3, and 302-4) can then be exposed when depositing the anode conductive layer 304. Thus, instead of a narrow contact area, this structure allows for a large anode contact area that connects to Schottky trench polysilicon layers as well as the trench MOSFET source terminal.

The second variation is in the number of adjacent trenches used to form the Schottky diode (306), a number that is strictly arbitrary. As shown in Figure 3, two parallel Schottky diode mesas 308 and 310 are formed between three trenches 302-2, 302-3, and 302-4. Since the area of the Schottky diode determines its forward voltage drop in response to current, Schottky structures with different numbers of adjacent trenches can be devised to arrive at the desired area. A two-mesa structure is shown in Figure 3 for illustrative purposes only, and the embodiment shown in Figure 3 could use a single mesa as in Figure 2, or more than two parallel mesas. Similarly, the embodiment shown in Figure 2 could use two or more parallel mesas to implement the Schottky diode. To better understand this aspect of the invention, Figures 5A and 5B provide simplified top views of the embodiments shown in Figures 2 and 3, respectively. In these drawings, an exemplary open-cell trench MOSFET process is assumed where trenches extend in parallel. Figure 5A illustrates nine trenches 500-1 to 500-9 where a single-mesa Schottky diode is provided between trenches 500-3 and 500-4 and another one is provided between trenches 500-7 and 500-8. An active trench MOSFET is formed between all other trenches. Figure 5B shows eight trenches 502-1 to 502-8 where a double-mesa Schottky diode is formed between trenches 502-3, 502-4, and 502-5. As shown in both figures the distance W between the Schottky trenches is smaller than the other inter-trench spacings.

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performance trade off is introduced by the method and structure of the present invention in that by enhancing the Schottky diode performance with a trench MOS structure, additional input capacitance is adversely incorporated into the MOSFET. This additional capacitance degrades the switching performance of the MOSFET to some extent. However, in many applications such a trade off is acceptable. For example, in the dc-dc converter application shown in Figure 1, switching loss in the lower transistor Q2 does not contribute that significantly to the overall conversion efficiency of the circuit.

In conclusion, the present invention provides methods and structure for a monolithically integrated Schottky diode and trench MOSFET. By distributing a Schottky diode within the cell array of the trench MOSFET, the overall switching characteristics of the MOSFET body diode is improved. While the above is a complete description of specific embodiments of the present invention, it is possible to use various alternatives, modifications and equivalents. For example, the techniques taught by the present invention can be employed in trench processes using either an open-call or a closed-cell structure. Therefore, the scope of the present invention should be determined not with reference to the above description but should, instead, be determined with reference to the appended claims, along with their full scope of equivalents.

WHAT IS CLAIMED IS:

1. A monolithically integrated structure combining a field effect transistor and a Schottky diode on a semiconductor substrate, comprising:

a first trench extending into the substrate and substantially filled by conductive material forming a gate electrode of the field effect transistor;

a pair of doped source regions positioned adjacent to and on opposite sides of the trench and inside a doped body region, the doped source regions forming a source electrode of the field effect transistor, and the substrate forming a drain electrode of the field effect transistor; and

a Schottky diode having a barrier layer formed on the surface of the substrate and between a pair of adjacent trenches extending into the substrate, the pair of adjacent trenches being substantially filled by conductive material and being separated by a distance W.

2. The monolithically integrated structure of claim 1 wherein the conductive material in each trench is separated from trench walls by a thin layer of dielectric.

3. The monolithically integrated structure of claim 2 further comprising a second trench adjacent to the first trench, the second trench forming the gate electrode of the field effect transistor in a similar fashion to the first trench,

wherein, a distance between the first trench and the second trench is greater than the distance W.

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1. A monolithically integrated structure combining a field effect transistor and a Schottky diode on a semiconductor substrate, comprising:

a first trench extending into the substrate and substantially filled by conductive material forming a gate electrode of the field effect transistor;

a pair of doped source regions positioned adjacent to and on opposite sides of the trench and inside a doped body region, the doped source regions forming a source electrode of the field effect transistor, and the substrate forming a drain electrode of the field effect transistor; and

a Schottky diode having a barrier layer formed on the surface of the substrate and between a pair of adjacent trenches extending into the substrate, the pair of adjacent trenches being substantially filled by conductive material and being separated by a distance W.

2. The monolithically integrated structure of claim 1 wherein the conductive material in each trench is separated from trench walls by a thin layer of dielectric.

3. The monolithically integrated structure of claim 2 further comprising a second trench adjacent to the first trench, the second trench forming the gate electrode of the field effect transistor in a similar fashion to the first trench,

wherein, a distance between the first trench and the second trench is greater than the distance W.

4. The monolithically integrated structure of claim 3 wherein the barrier layer comprises metal and electrically connects to the source electrode of the field effect transistor.

5. The monolithically integrated structure of claim 4 wherein the barrier layer and a metal layer connecting to the source regions comprise one of either titanium tungsten or titanium nitride.

6. The monolithically integrated structure of claim 5 wherein the barrier layer and the metal layer connecting to the source regions connect together by an overlying layer of aluminum.

7. The monolithically integrated structure of claim 4 wherein the conductive material in the first and second trenches electrically connects to the conductive material in the pair of adjacent trenches between which the Schottky diode is formed.

8. The monolithically integrated structure of claim 4 wherein the conductive material in the pair of adjacent trenches between which the Schottky diode is formed is electrically isolated from the conductive material in the first and second trenches.

9. The monolithically integrated structure of claim 8 wherein the metal forming the barrier layer also covers and connects to the conductive material in the pair of adjacent trenches between which the Schottky diode is formed.

10. The monolithically integrated structure of claim 8 wherein the conductive material in the pair of adjacent trenches between which the Schottky diode is formed, is recessed into the pair of adjacent trenches and covered by a layer of dielectric material.

11. A monolithically integrated structure combining a field effect transistor and a Schottky diode on a semiconductor substrate, comprising

a plurality of trenches extending in parallel and into the substrate forming a corresponding plurality of mesas therebetween, the plurality of trenches being substantially filled by a conductive material that is separated from trench walls by a thin layer of dielectric material;

a doped well region formed inside the plurality of mesas except for at least one mesa;

a pair of doped source regions formed on the surface of the substrate in each doped well region and adjacent to trench walls; and

a layer of metal formed on the surface of the substrate on the plurality of mesas to connect to the pair of doped source regions, the layer of metal also forming a barrier layer on the surface of the at least one mesa,

wherein, the layer of metal connecting to the pair of doped source regions forms a source terminal of the field effect transistor, the substrate forms a drain terminal of the field effect transistor, and the conductive material in the plurality of trenches forms a gate terminal of the field effect transistor, and

wherein, the layer of metal forming a barrier layer on the surface of the at least one mesa comprises an anode terminal of a Schottky diode and the substrate forms a cathode terminal of the Schottky diode.

12. The monolithically integrated structure of claim 11 wherein a width of the at least one mesa is smaller than a width of the remaining plurality of mesas.

13. The monolithically integrated structure of claim 12 wherein the conductive material substantially filling the plurality of trenches comprises polysilicon, and the layer of metal comprises titanium tungsten.

14. The monolithically integrated structure of claim 12 wherein the conductive material substantially filling the plurality of trenches are electrically connected.

15. The monolithically integrated structure of claim 12 wherein the conductive material inside trenches forming the at least one mesa is electrically isolated from conductive material inside the remaining plurality of trenches.

16. The monolithically integrated structure of claim 15 wherein the conductive material inside trenches forming the at least one mesa is electrically connected to the source terminal of the field effect transistor.

17. The monolithically integrated structure of claim 16 wherein the conductive material inside trenches forming the at least one mesa is recessed into the trench and covered by a layer of dielectric material.

20. A method of manufacturing a trench field effect transistor and a Schottky diode on a semiconductor substrate, comprising the steps of:

forming a plurality of trenches extending into the substrate, with a first trench being adjacent to a second trench, and the second being adjacent to a third trench;

forming a layer of conductive material inside the plurality of trenches, the layer of conductive material being isolated from trench walls by a dielectric layer;

forming a doped body region extending into the substrate between the first and the second trenches and not between the second and the third trenches;

forming doped source regions inside the doped body region and adjacent to the walls of the first and the second trenches; and

forming a conductive anode layer on the surface of the substrate between the second and the third trenches,

whereby a field effect transistor is formed with the substrate providing a drain terminal, the doped source regions a source terminal and the conductive layer in the first and the second trenches a gate terminal, and

a Schottky diode is formed with the substrate providing a cathode terminal and the conductive anode layer providing an anode terminal.

21. A method of manufacturing a trench field effect transistor and a Schottky diode on a semiconductor substrate, comprising the steps of:

forming a plurality of trenches extending into the substrate;

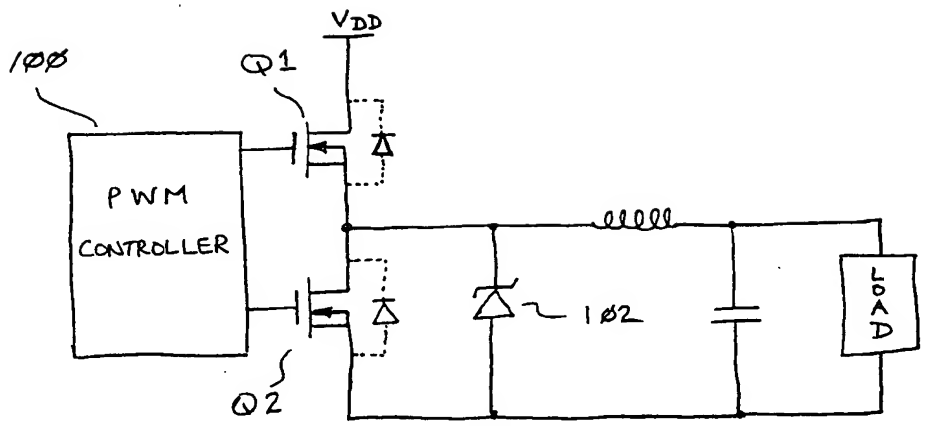
forming a layer of conductive material inside the plurality of trenches, the layer of conductive material being isolated from trench walls by a dielectric layer;

forming a plurality of doped body regions extending into the substrate between each adjacent pair of trenches;

forming doped source regions inside the doped body regions and adjacent to the walls of the adjacent pair of trenches; and

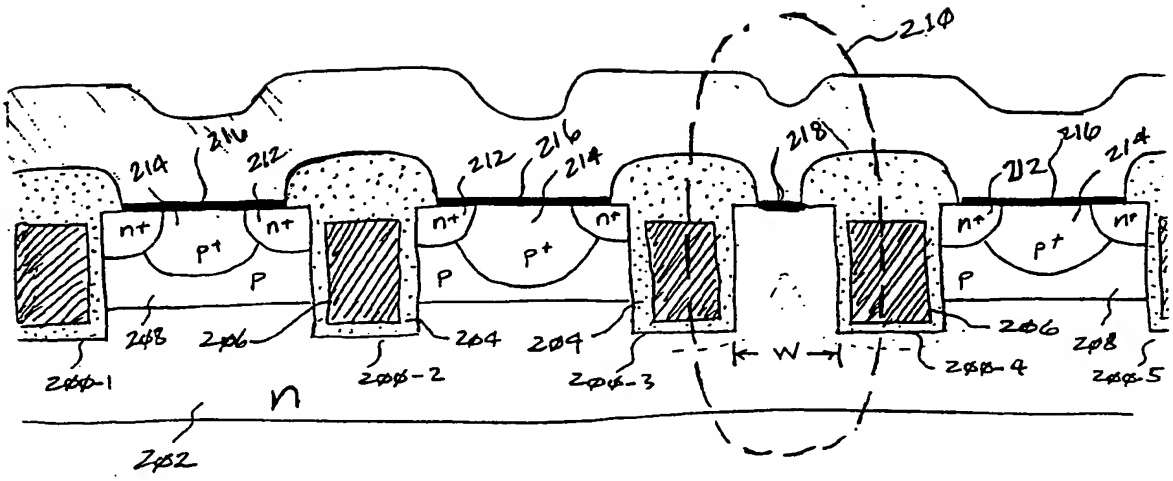
forming a conductive anode layer on the surface of the substrate between the plurality of doped body regions,

whereby an interspersed field effect transistor-Schottky diode structure is formed with the substrate providing a drain terminal, the doped source regions a source terminal and the conductive layer in the first and the second trenches a gate terminal of the field effect transistor, and the substrate providing a cathode terminal and the conductive anode layer providing an anode terminal of the Schottky diode.

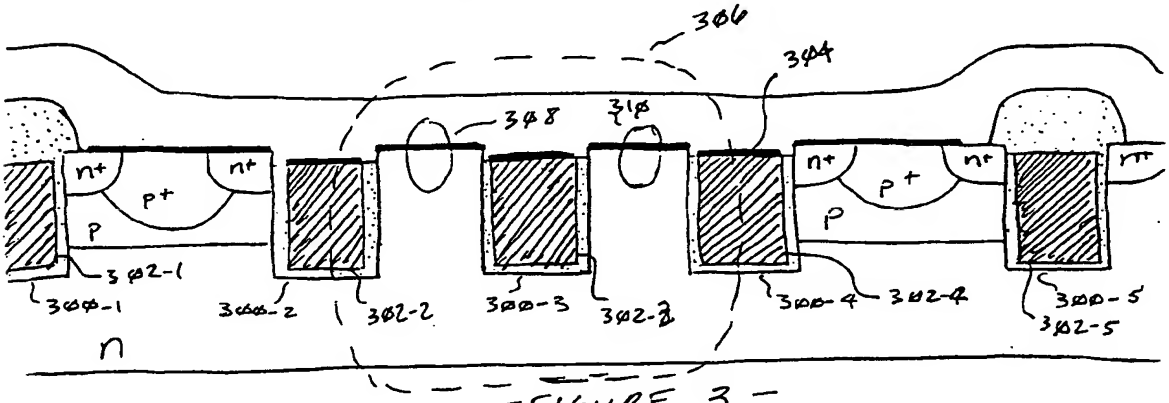


- FIGURE 1 -

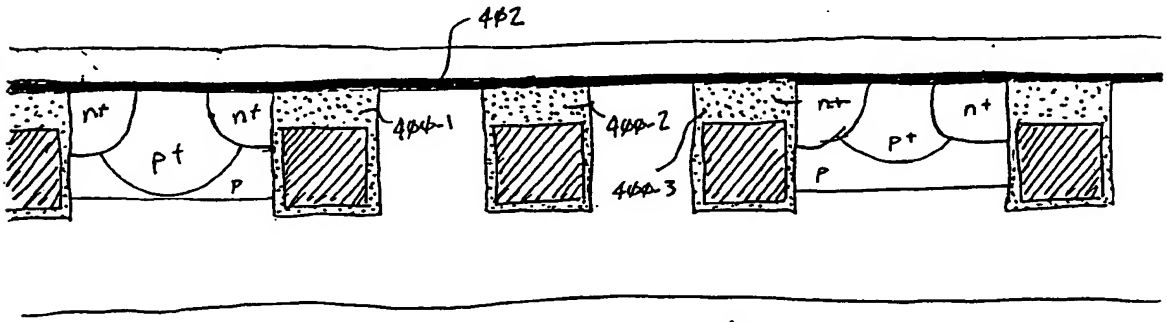
(PRIOR ART)



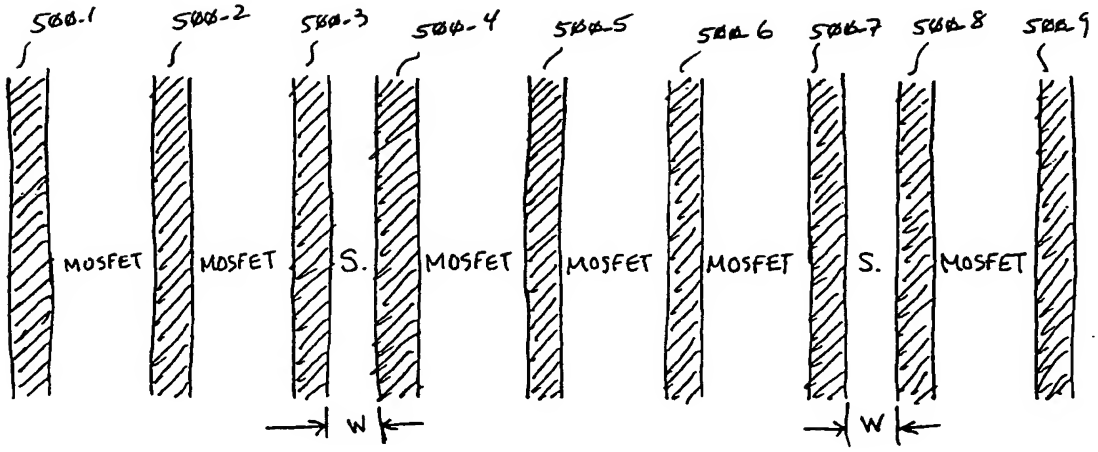
-FIGURE 2-



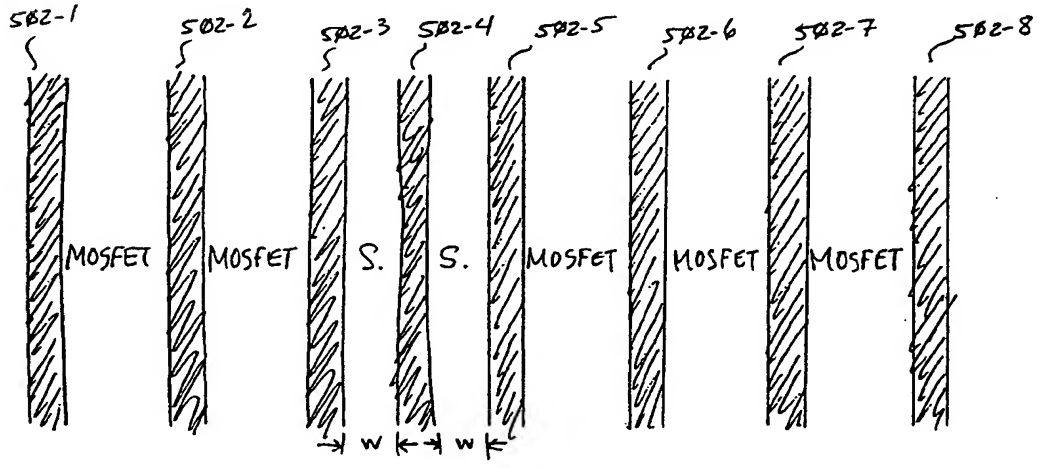
-FIGURE 3-



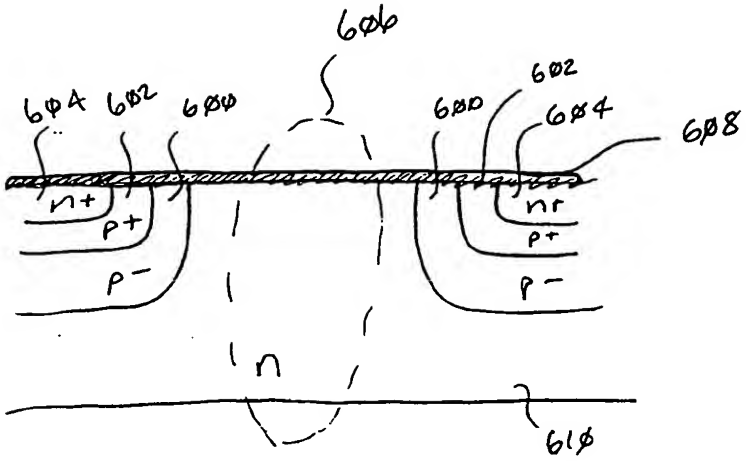
-FIGURE 4-



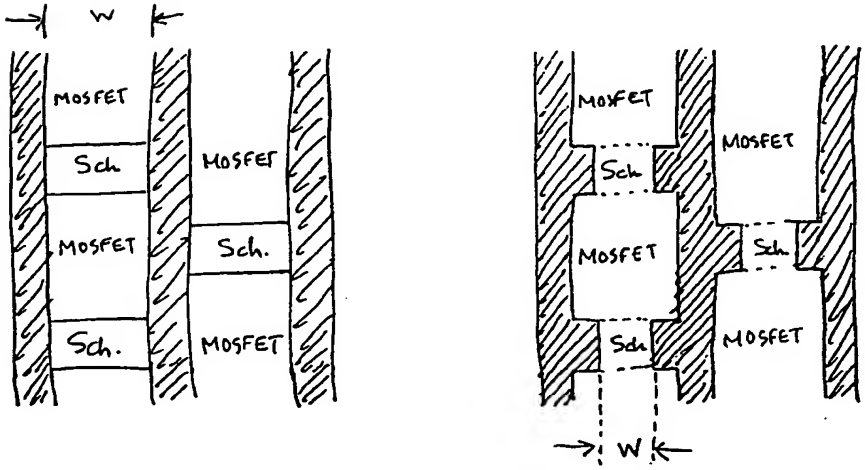
- FIGURE 5A -



- FIGURE 5B -



- FIGURE 6 -



- FIGURE 7A -